Design of Fixed and Programmable Counters Using the RCA CD4018 COS/MOS Presettable Divide-by-"N" Counter

by J. Litus Jr.

The RCA CD4018* COS/MOS (Complementary-Symmetry Metal-Oxide-Semiconductor) presettable divide-by-"N" counter is designed for use in digital equipment where low power dissipation, low package count, and high noise immunity are primary design requirements. The counter is particularly useful in such systems applications as channel-preset counters in digital frequency synthesizers and program-counter control. The CD4018 can also be used as a 5-stage parallel input/output holding register. In this application the parallel entry can be controlled by the preset-enable line to perform a 5-stage "latch" operation. This Note describes the use of the CD4018 in single-decade and multi-decade fixed and programmable divide-by-"N" counters. System considerations such as switch simplifications, components minimization, and speed are also discussed.

The logic diagram for the CD4018 is shown in Fig. 1. Fig. 2 shows the counting sequence and timing diagram for this device connected as a decade counter.

Supplied in plastic dual-in-line package as the CD4018E, in ceramic dual-in-line package as the CD4018D and in ceramic flat-pack as the CD4018.

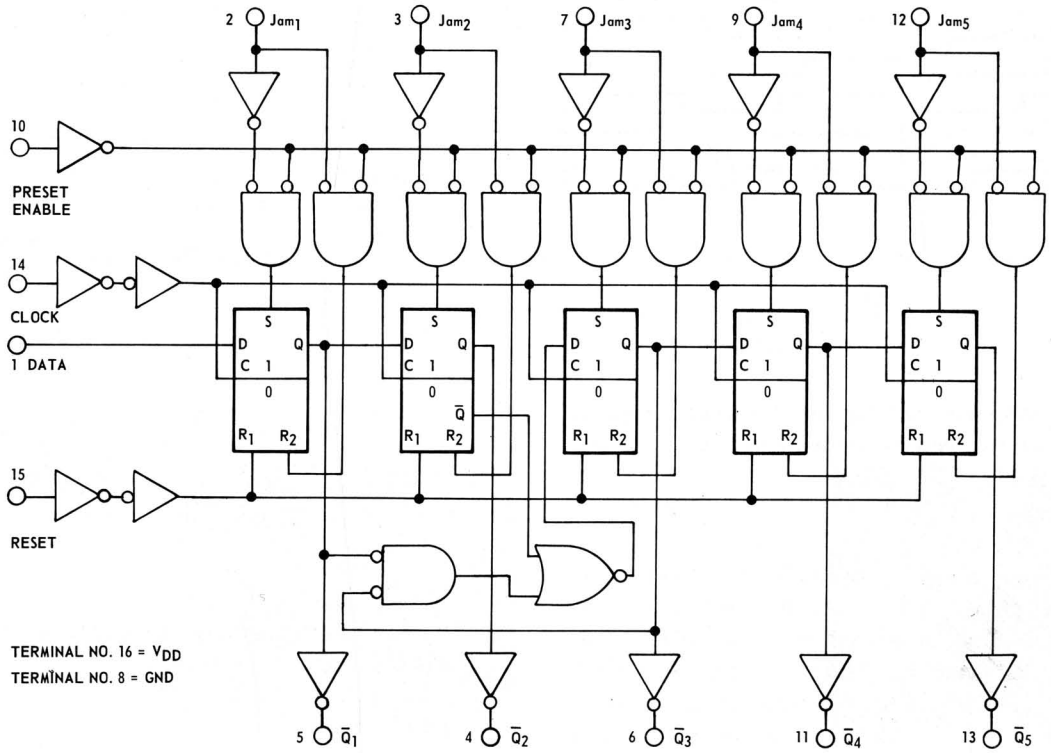

Fig. 1 - Logic diagram for CD4018.

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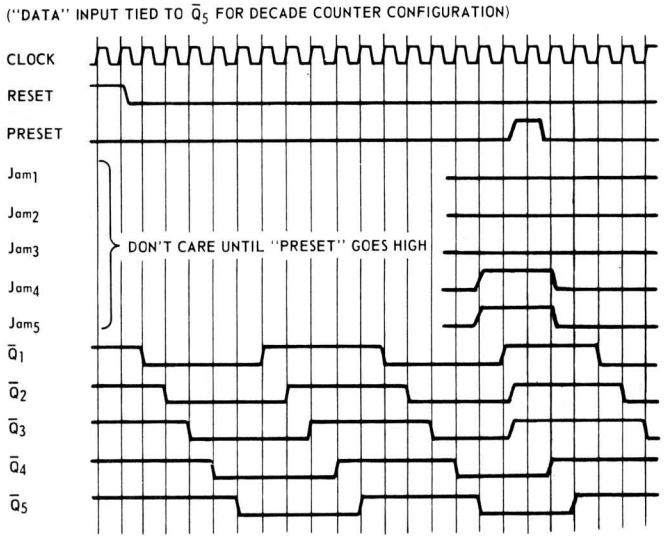
Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$
0	1	1	1	1	1
1	0	1	1	1	1
2	0	0	1	1	1
3	0	0	0	1	1
4	0	0	0	0	1
5	0	0	0	0	0
6	1	0	0	0	0
7	1	1	0	0	0
8	1	1	1	0	0
9	1	1	1	1	0

(a)



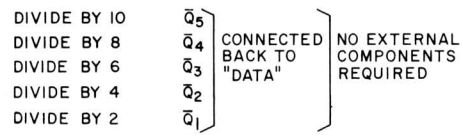
(b)

Fig. 2 - (a) counting sequence for decade-counter operation; (b) timing diagram for decade-counter operation.

The CD4018 consists of five flip-flops that can be connected as a five-, four-, three-, or two-stage Johnson Counter with buffered $\overline{Q}$ outputs from each stage. Gating is included for presetting the counter. "Clock", "Reset", "Data", "Preset-Enable", and five "Jam" inputs are also provided. The counter is advanced one count at the positive-going transition of the clock. A "high" Reset signal clears the counter to an "all-zero" ($\overline{Q}$ outputs are all "ones") condition, and a "high" Preset Enable signal allows information on the Jam inputs to preset the counter.

FIXED SINGLE-STAGE DIVIDE-BY-"N" COUNTERS

Divide-by-10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, or $\overline{Q}1$ signals, respectively, back to the Data input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of NOR- or NAND- gate packages to gate the proper feedback connection to the Data input line. Fig. 3 shows the feedback connections for divide-by-9, 7, 5, and 3 functions using the CD4011 NAND gate as the feedback circuit.



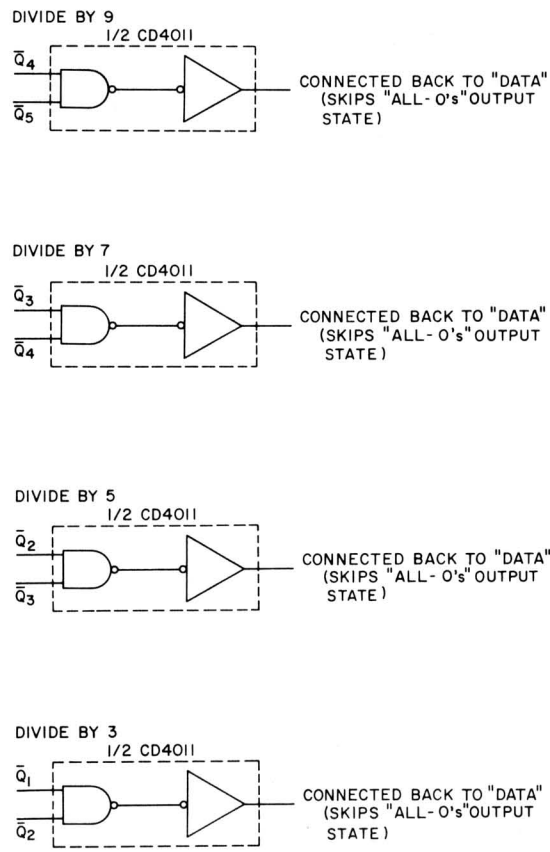
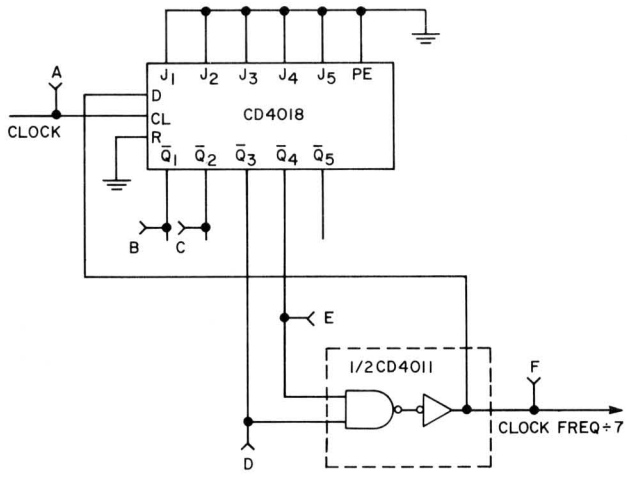
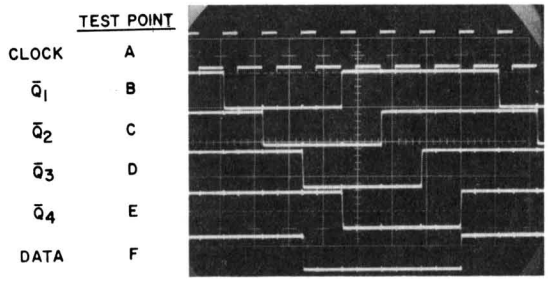


Fig. 3 - External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, and 2 operation.

Fig. 4 shows the divide-by-seven configuration in detail. The logic diagram and pertinent waveforms are shown in Figs. 4a and b. Fig. 4c shows the counting sequences for a divide-by-eight and a divide-by-seven configuration. Division



(a)



(b)

Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	0	0	0	0
5	1	0	0	0
6	1	1	0	0
7	1	1	1	0

Count	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$
0	1	1	1	1
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	1	1	0	0
6	1	1	1	0

(c)

Fig. 4 - CD4018 in a fixed divide-by-7 counter configuration: (a) logic diagram; (b) timing waveforms; (c) counting sequences for a ÷8 and a ÷7 Johnson Counter.

of the clock frequency by seven is accomplished by altering the counting sequence so as to skip the "all zeros" state of a divide-by-eight counter. The divide-by-seven counting sequence proceeds as in a normal 4-stage Johnson counter until count 3 (0001) at which point $\overline{Q}3=0$ and $\overline{Q}4=1$. At this point the CD4011 gates $\overline{Q}3$ and $\overline{Q}4$ to put a 0 on the Data input to the first stage. Thus, count 4 will be 1000 instead of 0000 as in the unaltered divide-by-eight sequence. The remainder of the counting sequence proceeds in the normal 4-stage manner.

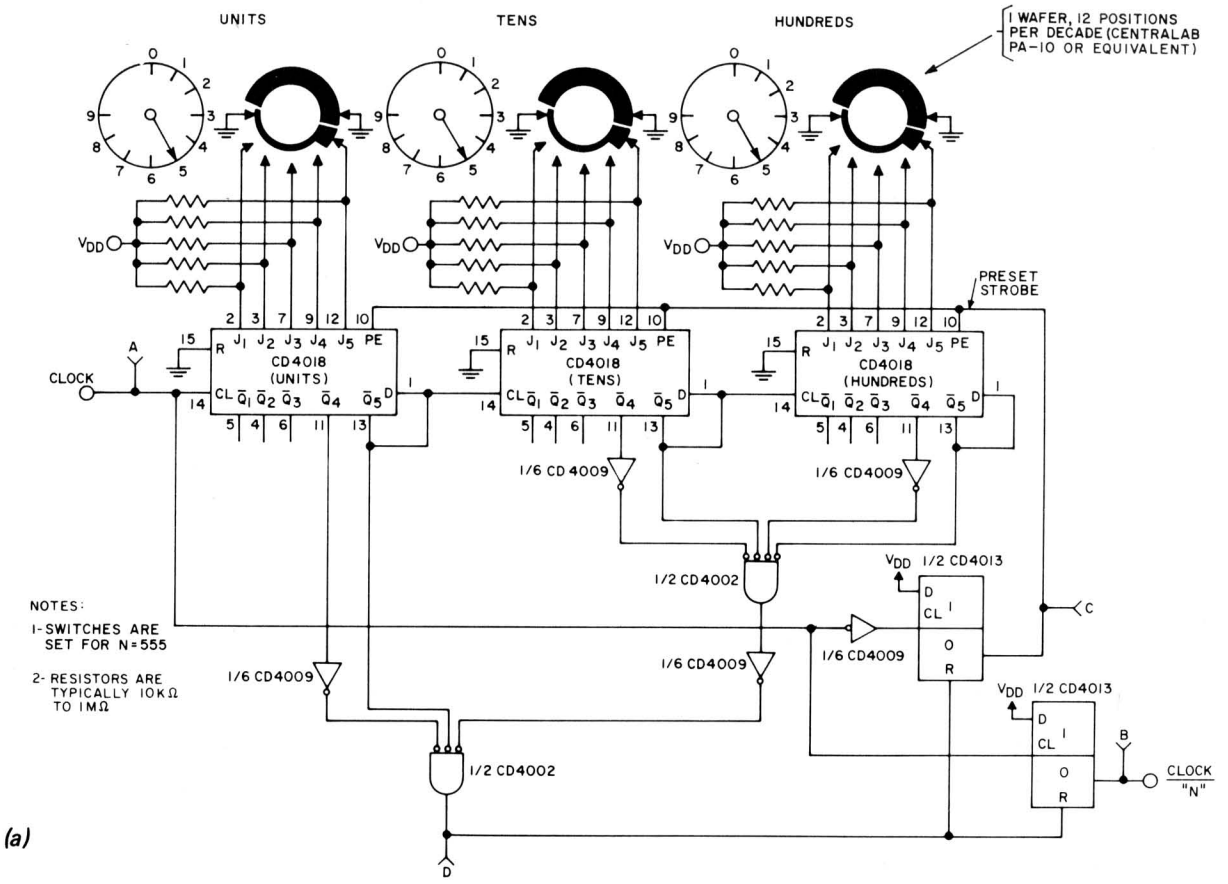
PROGRAMMABLE MULTI-DECADE DIVIDE-BY-"N" COUNTERS

The CD4018 is especially useful in applications requiring low-power, programmable, divide-by-"N" counting. Two such applications are channel preset counters in digital frequency synthesizers and program counter control.

Fig. 5 illustrates the use of three CD4018 units in a programmable divide by "N" counter, where "N" may be any number from 2 to 999 (counter output is equal to clock frequency divided by N). Extension to higher "N" ranges is readily accomplished by the use of additional CD4018 units. The counter is preset to the value of "N" via the three selector switches. The switches are arranged so that switch position 9 is equivalent to a "0" count in the counter, position 8 is equivalent to a "1" count, position 7 to a "2" count, etc. The counter counts up from the preset value (the N value) to its maximum count (999) and recycles, starting again from the preset value. Fig. 5b shows the counting sequence; oscillograph photographs of the waveform at various points in the circuit (of Fig. 5a) are shown in Fig. 5c. Fig. 5d shows the N-counter output for various values of N.

The Johnson-Counter configuration utilized in the CD4018 design permits significantly simpler "program-switch" ("N"-Select) implementation than is required in systems that use a BCD decade counter arrangement. The program switch is composed of three standard single-wafer switches, one for each CD4018 (one per decade). This compares with a four-wafer (4-pole) switch per decade for a BCD decade-counter arrangement. Also, the count decoding is much simpler in that only two outputs per CD4018 must be decoded as compared to four for a BCD arrangement. The Johnson-type counter can also operate at higher speeds and provides spike-free decoded outputs.

The configuration shown in Fig. 5 permits frequency division by 2 as a result of performing the Preset function during half a clock cycle. In this mode the maximum allowable frequency of operation is reduced, however. If this reduction in frequency is not acceptable, the logic diagram shown in Fig. 6 can be employed. In this circuit the Preset function is allowed a full clock cycle but the range of frequency division is reduced to 3 to 999. The counting sequence and pertinent timing waveforms for this circuit are shown in Figs. 6b, c, and d, respectively. Typical maximum operating frequency is 2 megahertz, for the counter in Fig. 5 and 3 megahertz for the counter in Fig. 6.



(a)

FIRST DECADE (UNITS)

SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0 *

SECOND DECADE (TENS)

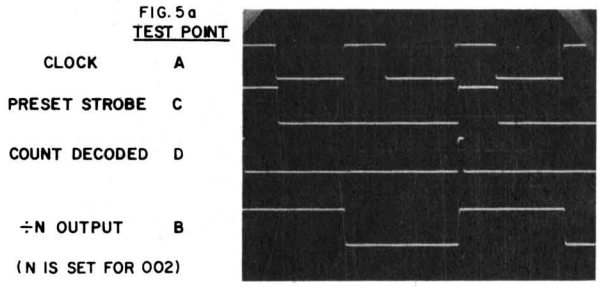
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0 *

THIRD DECADE (HUNDREDS)

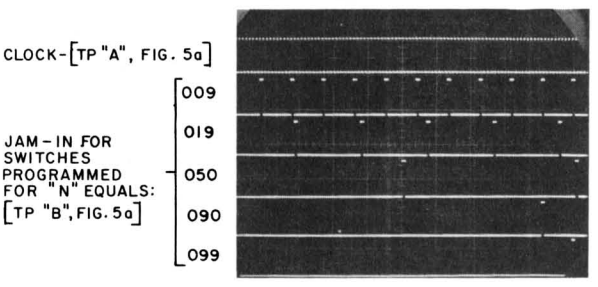
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1
8	1	0	1	1	1	1
7	2	0	0	1	1	1
6	3	0	0	0	1	1
5	4	0	0	0	0	1
4	5	0	0	0	0	0
3	6	1	0	0	0	0
2	7	1	1	0	0	0
1	8	1	1	1	0	0
0	9	1	1	1	1	0 *

(b)

*These digits, representative of count "9" in each decade, are decoded to give the preset strobe

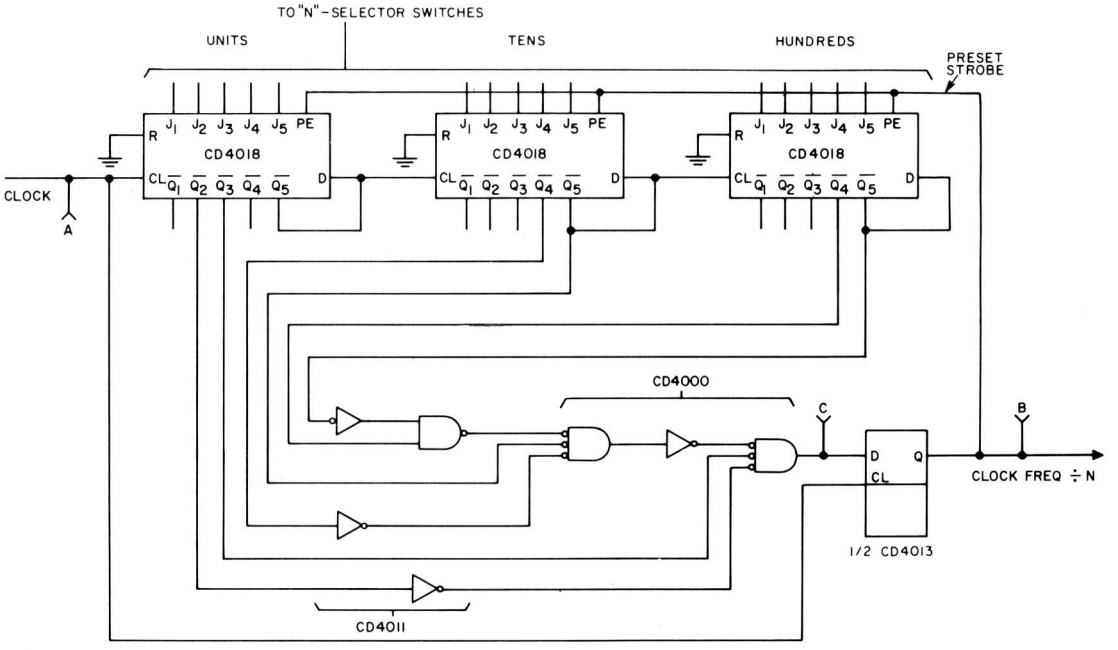


(c)



(d)

Fig. 5 — Three-decade, programmable, divide-by-"N" counter with frequency division from 2 to 999: (a) logic diagram; (b) counting sequence; (c) timing waveforms at various points in the circuit (d) ÷N output for various values of N.

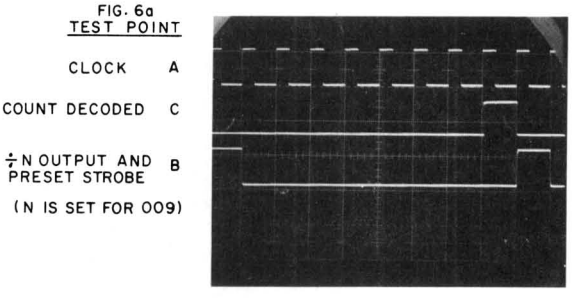


(a)

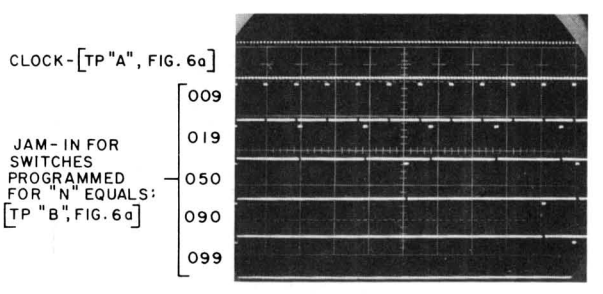
FIRST DECADE (UNITS)							SECOND DECADE (TENS)							THIRD DECADE (HUNDREDS)						
SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	SW. POS. N	Count	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$
9	0	1	1	1	1	1	9	0	1	1	1	1	1	9	0	1	1	1	1	1
8	1	0	1	1	1	1	8	1	0	1	1	1	1	8	1	0	1	1	1	1
7	2	0	0	1	1	1	7	2	0	0	1	1	1	7	2	0	0	1	1	1
6	3	0	0	0	1	1	6	3	0	0	0	1	1	6	3	0	0	0	1	1
5	4	0	0	0	0	1	5	4	0	0	0	0	1	5	4	0	0	0	0	1
4	5	0	0	0	0	0	4	5	0	0	0	0	0	4	5	0	0	0	0	0
3	6	1	0	0	0	0	3	6	1	0	0	0	0	3	6	1	0	0	0	0
2	7	1	1	0	0	0	2	7	1	1	0	0	0	2	7	1	1	0	0	0
1	8	1	1	1	0	0	1	8	1	1	1	0	0	1	8	1	1	1	0	0
0	9	1	1	1	1	0	0	9	1	1	1	1	0	0	9	1	1	1	1	0

NOTE: "N" IS SELECTED BY DIALING IN THE DESIRED PRESET COUNT INDICATED BY THE SWITCH SETTINGS: THE "9" COUNTS FROM THE SECOND AND THIRD DECADE (SHOWN AS [1][0]) ARE GATED WITH THE "7" COUNT (SHOWN AS [1][0]) FROM THE FIRST DECADE TO ACTIVATE THE "PRESET ENABLE", ONCE PER COUNTER CYCLE.

(b)



(c)



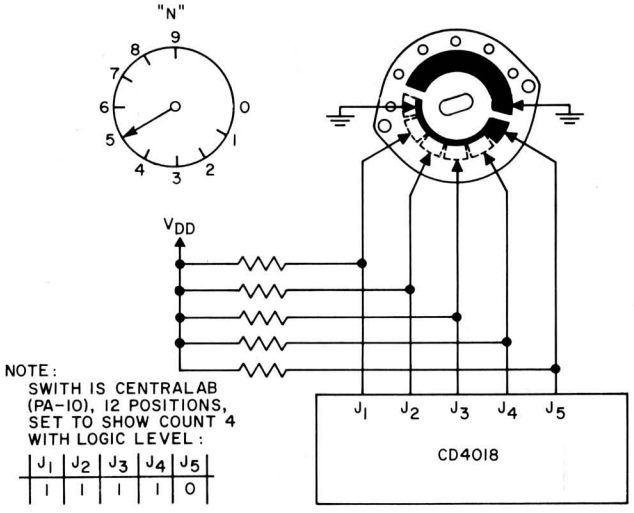
(d)

Fig. 6 — Three-decade, programmable, divide-by-"N" counter with frequency division from 3 to 999: (a) logic diagram; (b) counting sequence; (c) timing waveforms at various points in the circuit; (d) divide-by-N output for various values of N.

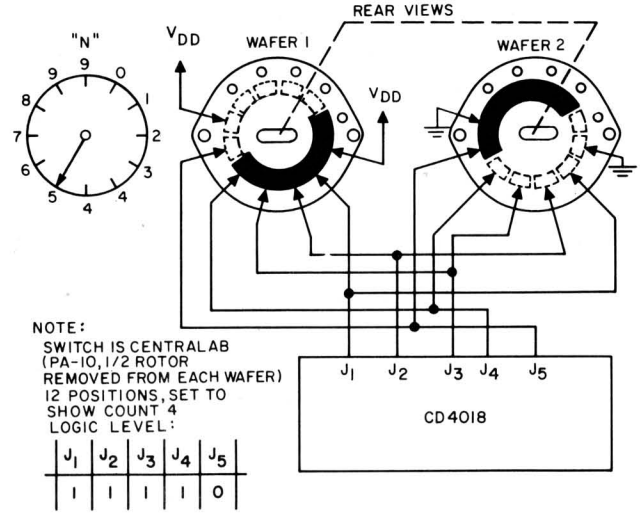
PROGRAM-SWITCH ("N"-SELECT) OPTIONS

Fig. 7a is a detailed drawing of a standard Centralab 12-position wafer switch and the associated resistor network as used in Fig. 5a. The resistors connected to V_{DD} are required to prevent floating inputs on the "JAM" lines. In applications that require lower power dissipations or where component count or space considerations become important, the resistor network can be eliminated by the redesign of the switch. Two such options are shown in Figs. 7b and 7c.

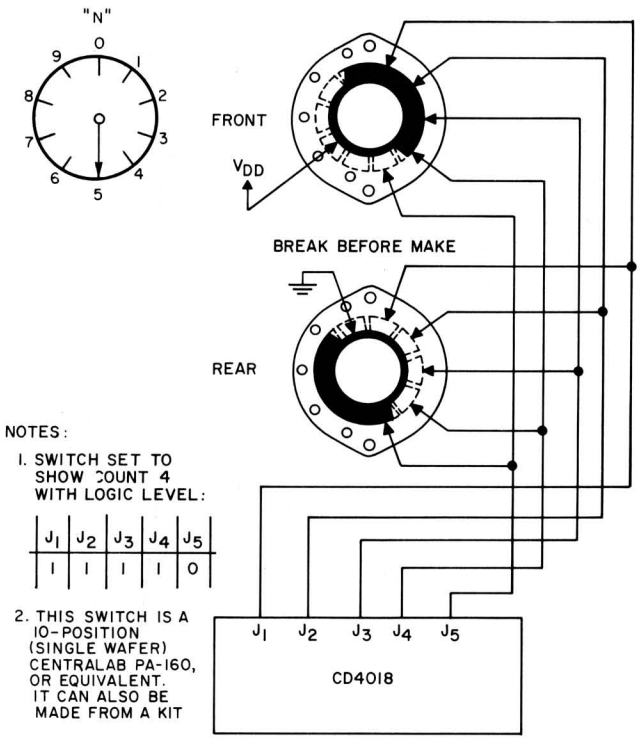
As previously mentioned in the discussion of Fig. 5, the range of N can be extended by adding more CD4018 units. In addition to this type of expansion each stage in the programmable divide-by-N counter can be designed to count to any base or radix. For example, the single stage divide-by-seven counter of Fig. 4 may be used as each stage in a multi-stage programmable counter.



(a)



(b)



(c)

Fig. 7 - Switch configurations; (a) single wafer (standard) per decade; (b) two wafers (modified standard) per decade; (c) single wafer (nonstandard) per decade.

SUMMARY

The RCA CD4018 is a versatile counter. Because of the Johnson-Counter design employed, this device permits the design of simple decoding and preset switching circuits. The system can also operate at higher speeds and with much less power dissipation than a comparable BCD decade counter arrangement. Also the CD4018, a COS/MOS device, possesses all the inherent advantages of this technology.

This versatile device can be used in fixed or programmable divide-by-"N" counters where "N" can vary from two to ten for a single CD4018 and greater than ten for multiple CD4018 stages. From an economical viewpoint, its versatility and low power requirement at high speeds make the RCA CD4018 the logical choice for counter applications in control and frequency synthesization equipments.